IJC-4 JTAG Programming Cable

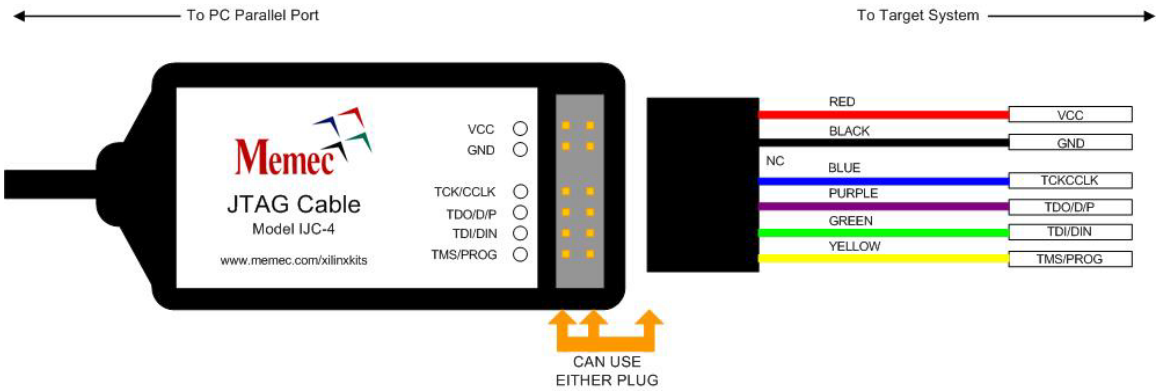
The IJC-4 JTAG Cable from Memec Design is a PC-only based cable that attaches to the PC parallel port on one end and has a 6 lead attachment on the other to connect to the target FPGA/CPLD device(s) being programmed. The JTAG cable supports iMPACT in boundary scan mode and slave serial mode, as well as ChipScope and XMD/GDB. The cable will support JTAG programming in 5V, 3.3V and 2.5V programming modes.

The table below shows the signal definitions for each of the programming modes supported.

Name	Function
JTAG Leads (Boundary Scan)	
VCC	Power - Supplies 2.5V to 5V to the cable.
GND	Ground - Supplies ground reference to the cable.
TCK	Test Clock - Drives the test logic for all devices on a JTAG chain.
TDO	Test Data Output - data from the target system is read at this pin.
TDI	Test Data Input - this signal is used to transmit serial test instructions and data.
TMS	Test Mode Select - this signal is decoded by the JTAG state machine to control test operations.

FPGA Leads (Slave Serial)	
VCC	Power-Supplies 2.5V to 5V to the cable.
GND	Ground-Supplies ground reference to the cable.
CCLK	Configuration Clock-Provides the clock during configuration or readback.
D/P	Done-Indicates when configuration is complete.
DIN	Data In-Provides configuration data during configuration.
PROG	Program-Provides program pulse causing the FPGA to configure.

The following figure shows how to connect the fly lead adapter to the cable box. Either row of headers may be used to connect to the fly lead adapter, since the cable signals are routed to both strips. Be sure to align the red VCC end of the connector with the top VCC position on the cable.



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